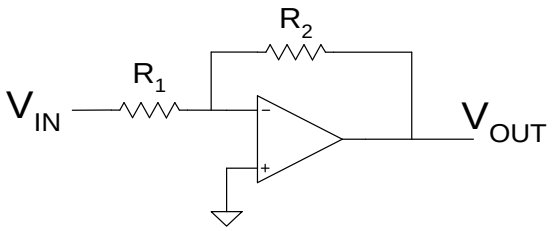
EE 505
Homework 3
Spring 2025

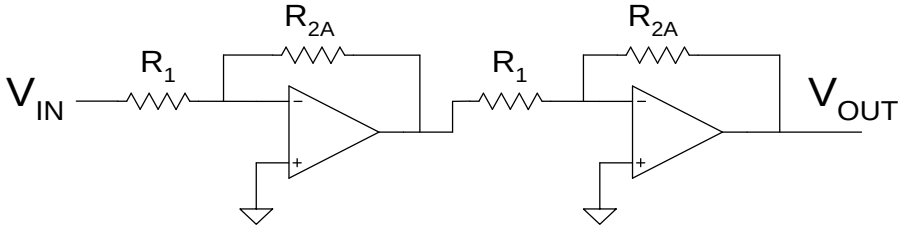
Due Friday March 14

Problem 1 An amplifiers is shown that has been designed for a gain magnitude of 16. Assume the Pelgrom parameter A_R characterizes the matching characteristics of the resistors and the total area of R_1 and R_2 is A_{TOT}. The performance requirements for an amplifier to be classified as good at production test is a gain that is within 1% of the nominal gain of 16. Assume the op amp has an arbitrarily high voltage gain and neglect any contact resistance and gradient effects.



a) If 16 equal-sized resistors are used to realize R_2 and one resistor of the same size is used to realize R_1 and the total resistor area is 170μm^2, determine the Pelgrom parameter A_R if the yield at test is 95%.
b) If 16 equal-sized resistors are placed in parallel to realize R_1 and a single resistor is used to realize R_2, determine the yield assuming the total resistor area is the same as that used in part a) and compare the results that were obtained for Part a).
c) If 4 equal-sized resistors are placed in series to realize R_2 and 4 resistors of the same size are placed in parallel to realize R_1, determine the yield assuming the total resistor area is the same as that used in part a) and compare the results with the previous structures.
d) If 60 equal sized resistors are placed in a series-parallel combination by placing the series connection of 30 resistors in parallel with a second series connection of 30 resistors and if this is placed in series with a single resistor of the same size to realize R_2 and if a single equal-sized resistor is used to realize R_1, determine the yield assuming the total resistor area is the same as that used in part a) and compare the results with the previous structures.

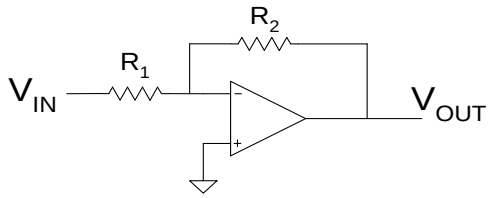
Problem 2 An alternative way to realize the gain that has a magnitude of 16 is to cascade two amplifiers in series as shown below.



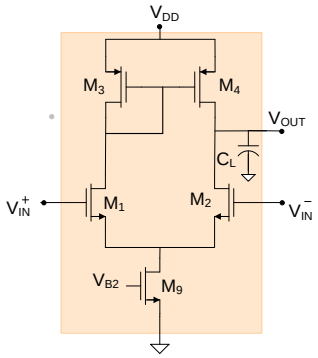
a) Compare the yield of the cascade amplifiers with that of the realizations in Problem 1 if the two finite gain amplifiers are identical and if the R_{2A} resistors are comprised of four unit resistors connected in series and R_1 is a single identical unit resistor. Assume the total area for the resistors is the same as in Problem 1.

b) Repeat part a) if the R_{2A} resistors are two unit resistors connected in series and the R_1 resistors are two unit resistors connected in parallel. Compare the yield of the cascaded amplifiers with that of the realizations in Problem 1 and Problem 2 if the area of the unit resistor used to realize R_1 in the cascade is increased so that the total resistor area in the cascade is identical to that of the resistors in Problem 1.

Problem 3 If the total area is fixed, determine how the relative area should be allocated between R_1 and R_2 in the following circuit to maximize the yield for a given closed loop gain of K. The determination should include a mathematical justification for any conclusions you draw.



Problem 4 From whatever PDK you are most comfortable with, obtain values for the Pelgrom parameters A_{VTO}, A_μ and A_{COX} (or alternately A_{VT0} and A_β). Consider the following operational amplifier.



a) Assume in the design that the area allocated to the p-channel transistors is equal to that allocated to the n-channel resistors. Under this assumption, determine the total area for a 3σ value of the offset voltage of 10mV. Assume an excess bias on both the n-channel and p-channel devices of 200mV and a total power dissipation of 10mW. Neglect any gradient effects and any A_L and A_W effects.

b) How will the area change if the power dissipation is increased to 50mW?

c) What would be the 3σ value of the offset voltage if the n-channel transistors are minimum sized and the p-channel transistors are as small as possible using the same values for A_{VTO}, A_{μ} and A_{COX} ? As in part a) assume the excess bias on both the n-channel and p-channel devices of 200mV.

Problem 5 Determine the 3σ value of INL_{kmax} for a 12-bit string DAC if each of the resistors is 2μ wide and 6μ long. Assume A_R for the process is 0.01μm.

Problem 6 Size the resistors in Problem 6 for a yield of 95% if the magnitude of INK_{kmax} must be less than 2 LSB.

Problem 7 Derive an expression for the standard deviation of the DNL of a binary-weighted current steering DAC at the mid-point transition from <0111111111> to <1000000000>. Express this in terms of the normalized standard deviation of a unary current source $\sigma_{\frac{I_{UR}}{I_{Unom}}}$. Assume the DAC is realized by bundling these unary current sources into groups of $1,2,4,\ldots 2^{n-1}$.

Problem 6 Derive an expression for the offset voltage due to local random variations for a differential amplifier with a p-channel mirror load on the first stage if the n-channel input transistors have Fn fingers connected in parallel and if the p-channel mirror transistors have Fp fingers connected in parallel.